UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,085	03/29/2001	Jingsheng Jason Cong	004120.P005	6979

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EXAMINER
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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-16,20-27 and 31-33* is/are rejected.

7)☒ Claim(s) *6-8,17-19 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-33 of the application have been examined.

Information Disclosure Statement

2.   Acknowledgment is made of the information disclosure statements filed on July
17, 2001 and October 20, 2002 together with copies of the patents and papers. The
patents and papers have been considered in reviewing the claims.

Drawings

3.   The drawings are objected to; see a copy of Form PTO-948 for an explanation.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and
> distinctly claiming the subject matter which the applicant regards as his invention.

5.　　Claim 4, 5, 10, 15, 16, 21, 26, 27 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 15 and 26 use the relation $t_v \ln[(t_x - t_r v_t)(e_r^{t/t}{}_v - 1)/ t_r v_t]$, in which the variable t_x is not defined, making it impossible to compute. Therefore, it is not possible to compute the noise width.

Claims 10, 21 and 32 use the relation $(R_d + R_s) C_x / \{ R_d (C_1 + C_x + C_2 + C_L) + R_s (C_x + C_2 + C_L) + R_e C_L\}$ to compute the peak noise amplitude. However, the various variables used in this relation are not defined, making it impossible to compute.

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

Claim Rejections - 35 USC § 103

6.　　The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

8.   Claims 1, 2, 9, 12, 13, 20, 23, 24 and 31 are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Jin et al.** ("A new

approach to analyze interconnect delays in RC wire models", IEEE, 1999), and further in view of

Kahng et al. ("Noise models for multiple segmented RC interconnects", IEEE, 26-28 March,

2001).

8.1   **Aingaran et al.** teaches two pole coupling noise analysis model for submicron integrated

circuit design verification. Specifically, as per claim 23, **Aingaran et al.** teaches an apparatus for

identifying potential noise failures in an integrated circuit design (Abstract, L1-3; CL3, L48-53);

comprising:

        means for locating a victim net and an aggressor within the integrated circuit design

(Abstract, L5-8); and

        means for indicating that the integrated circuit design requires modification if modeling

the victim net indicates that a potential noise failure may occur in the integrated circuit design

(Abstract, L12-18).

Aingaran et al. teaches means for modeling the victim net using single π-type

resistor-capacitor (RC) circuits, including means for determining a coupling between the victim

net and the aggressor (CL5, L14-22). Aingaran et al. does not expressly teach means for

modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for

determining a coupling between the victim net and the aggressor. Jin et al. teaches means for

modeling the victim net using multiple π-type resistor-capacitor (RC) circuits (Page VI-247,

CL1, Para 3; Fig. 2; CL2, Para 2), as the accuracy of the RC lumped circuit models is dependent

on the number of sections used (Page VI-246, CL1, Para 1). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of

Aingaran et al. with the apparatus of Jin et al. that included means for modeling the victim net

using multiple π-type resistor-capacitor (RC) circuits. The artisan would have been motivated

because the accuracy of the RC lumped circuit models would be dependent on the number of

sections used.

Kahng et al. teaches means for modeling the victim net using three π-type

resistor-capacitor (RC) circuits, including means for determining a coupling between the victim

net and the aggressor and a means for modeling the victim net using two π-type

resistor-capacitor (RC) circuits, including means for determining a coupling between the victim

net and the aggressor (Page 147, CL1, Para 3; CL2, Fig. 3; CL2, Para 1 to Page 148, CL1, Para

1), as that would allow analyzing the segmented configuration of the interconnect, while

reducing the complexity of the analytical model and the analytical expressions for noise and

delay (Page 147, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at

the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus

of **Kahng et al.** that included a means for modeling the victim net using two π-type

resistor-capacitor (RC) circuits, including means for determining a coupling between the victim

net and the aggressor. The artisan would have been motivated because that would allow

analyzing the segmented configuration of the interconnect, while reducing the complexity of the

analytical model and the analytical expressions for noise and delay.

8.2   As per claim 24, **Aingaran et al., Jin et al.** and **Kahng et al.** teach the apparatus of claim

23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net using

two π-type resistor-capacitor (RC) circuits comprises means for modeling the victim net with one

π-type RC circuit before a coupling location and one π-type RC circuit after the coupling

location. **Kahng et al.** teaches that the means for modeling the victim net using two π-type

resistor-capacitor (RC) circuits comprises means for modeling the victim net with one π-type RC

circuit before a coupling location and one π-type RC circuit after the coupling location (Page

147, CL2, Fig. 3; Page 146, CL2, Para 3), as that would allow calculating victim wire resistance,

victim driver resistance, victim ground capacitance and coupling capacitance for different

configurations of the aggressor victim overlap and different lengths before and after the overlap

(Page 147, CL2, Para 1 to Page 148, CL1, Para 1; Page 146, CL2, Para 3). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

apparatus of **Aingaran et al.** with the apparatus of **Kahng et al.** that included the means for

modeling the victim net using two π-type resistor-capacitor (RC) circuits comprising means for

modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC

circuit after the coupling location. The artisan would have been motivated because that would allow calculating victim wire resistance, victim driver resistance, victim ground capacitance and coupling capacitance for different configurations of the aggressor victim overlap and different lengths before and after the overlap.

8.3   As per claim 31, **Aingaran et al., Jin et al.** and **Kahng et al.** teach the apparatus of claim 23. **Aingaran et al.** also teaches that the means for modeling the victim net comprises means for determining the peak noise amplitude (CL6, L50-56; CL10, L27-37).

8.4   As per Claims 1, 2, 9, 12, 13 and 20, these are rejected based on the same reasoning as Claims 23, 24 and 31, <u>supra.</u> Claims 1, 2, 9, 12, 13 and 20 are method and article of manufacture comprising one or more recordable medium claims reciting the same limitations as Claims 23, 24 and 31, as taught throughout by **Aingaran et al., Jin et al.** and **Kahng et al.**

9.   Claims 3, 14 and 25 are rejected under 35 U.S.C. 103(a) under 35 U.S.C. 103(a) as being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Jin et al.** ("A new approach to analyze interconnect delays in RC wire models", IEEE, 1999), and further in view of **Kahng et al.** ("Noise models for multiple segmented RC interconnects", IEEE, 26-28 March, 2001) and **Huang** (U.S. Patent 5,568,395).

9.1   As per claim 25, **Aingaran et al., Jin et al.** and **Kahng et al.** teach the apparatus of claim 23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net

comprises means for determining noise width. **Huang** teaches that the means for modeling the

victim net comprises means for determining noise width (CL20, L66 to CL21, L1), as false logic

error occurs when false logic noise height and noise width exceed the thresholds specified for the

particular technology (CL14, L34-40). It would have been obvious to one of ordinary skill in the

art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the

apparatus of **Huang** that included the means for modeling the victim net comprising means for

determining noise width. The artisan would have been motivated because false logic error

occurs when false logic noise height and noise width exceed the thresholds specified for the

particular technology.

9.2   As per Claims 3 and 14, these are rejected based on the same reasoning as Claim 25,

<u>supra.</u> Claims 3 and 14 are method and article of manufacture comprising one or more

recordable medium claims reciting the same limitations as Claim 25, as taught throughout by

Aingaran et al., Jin et al., Kahng et al. and **Huang.**

10.   Claims 11, 22 and 33 are rejected under 35 U.S.C. 103(a) under 35 U.S.C. 103(a) as

being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Jin et al.** ("A new

approach to analyze interconnect delays in RC wire models", IEEE, 1999), and further in view of

Kahng et al. ("Noise models for multiple segmented RC interconnects", IEEE, 26-28 March,

2001) and **Alpert et al.** (U.S. Patent 6,117,182).

10.1   As per claim 33, **Aingaran et al., Jin et al.** and **Kahng et al.** teach the apparatus of claim

23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net

comprises computing crosstalk noise at a sink with a lumped capacitance at each branch

incorporated on a path from a source to the sink, with lumped capacitances being added in a

weighted manner based on their locations on the path. **Alpert et al.** teaches that the means for

modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance

at each branch incorporated on a path from a source to the sink, with lumped capacitances being

added in a weighted manner based on their locations on the path (CL6, L52-60; CL10, L12-20),

because the net consists of a source and a sink; the aggressor net transmits aggressor pulse into

the victim net due to coupling capacitance which is proportional to the distance the aggressor net

and the victim net run parallel to each other (CL6, L52-60). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of

Aingaran et al. with the apparatus of **Alpert et al.** that included the means for modeling the

victim net comprising computing crosstalk noise at a sink with a lumped capacitance at each

branch incorporated on a path from a source to the sink, with lumped capacitances being added

in a weighted manner based on their locations on the path. The artisan would have been

motivated because the net would consist of a source and a sink; the aggressor net would transmit

aggressor pulse into the victim net due to coupling capacitance which would be proportional to

the distance the aggressor net and the victim net run parallel to each other.

10.2   As per Claims 11 and 22, these are rejected based on the same reasoning as Claim 33,

supra. Claims 11 and 22 are method and article of manufacture comprising one or more

recordable medium claims reciting the same limitations as Claim 33, as taught throughout by

Aingaran et al., Jin et al., Kahng et al. and **Alpert et al.**

Allowable Subject Matter

11. Claims 6-8, 17-19 and 28-30 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from
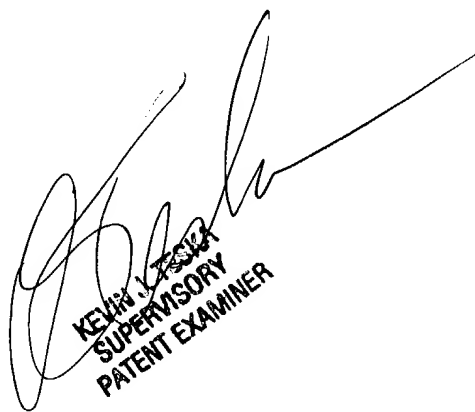
8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9600.

K. Thangavelu
Art Unit 2123
June 24, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER